CHAPTER

1 Introduction to Multilevel Inverters

LEARNING OBJECTIVES

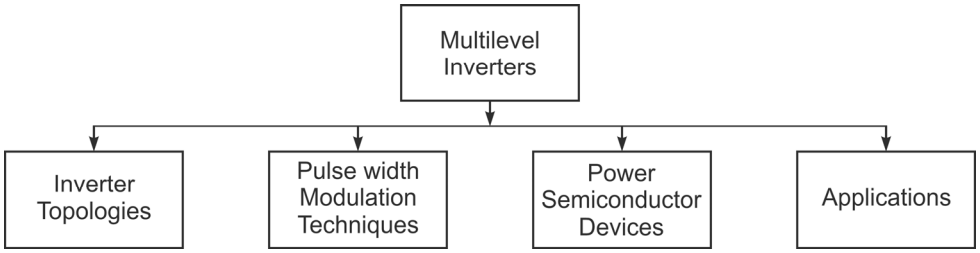
- ✓ *To understand and acquire knowledge about importance of multilevel inverters and its classification.*
- ✓ *To prepare learners to classify multilevel inverters.*
- ✓ *To prepare learners to classify basic pulse width modulation techniques.*
- ✓ *To recollect and remember the power semiconductor devices and their symbols for using them in multilevel inverters.*

1.1 Introduction

In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, Static VAR Compensators (STATCOMs), Flexible AC Transmission System (FACTS), high voltage direct current lines, electrical vehicle drives and renewable energy systems. The most attractive features of multilevel inverters are they can generate output voltages with extremely low distortion and lower dv/dt, increased power ratings, improved harmonic performance, and reduced electromagnetic interference (EMI) emission, draws input current with very low distortion that can be achieved with multiple dc levels that are synthesis of the output voltage waveform, and they generate smaller Common Mode (CM) voltage thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated. They can operate with a lower switching frequency.

There are numerous industrial applications requiring medium voltage and high-power converters. It is troublesome to achieve medium voltage and high power with directly connecting a single power semiconductor switch to the megawatt grid. For these reasons a new family of Multilevel Inverters has emerged as a solution for working with medium voltage and high-power ranges.

In this chapter the following topics are briefly discussed for Multilevel Inverters, such as various Inverter topologies, various pulse width modulation techniques, various types of power semiconductor devices and their applications.



The general structure of the multilevel inverters is to synthesize a sinusoidal voltage from several small levels of voltages, typically obtained from capacitor voltage sources. The multilevel starts from three-level. The waveform obtained from a three-level inverter is a quasi-square wave output. As the number of levels increases, the synthesized output waveform adds more steps producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. Ultimately, a zero-harmonic distortion of the output wave can be achieved by an infinite number of levels. More levels also mean higher voltages can be achieved by connecting several switching devices in series, which inherently pose device voltage sharing problems. The voltage unbalance problem can be solved by replacing capacitor by a constant dc voltage source.

The multilevel inverters are used to minimize the output voltage distortion with improved fundamental voltage and also due to good power quality, low switching losses, high voltage capability and good electromagnetic compatibility (EMC).

The main disadvantages of multilevel inverters are that they require large number of switching devices at lower voltages and small voltage steps are supplied on the dc input side. The multilevel inverters provide more than two voltage levels and as the number of levels increases, the output total harmonic distortion decreases, resulting to sinusoidal waveform.

Table 1.1 Comparison of conventional two-level inverter and multilevel inverter.

Serial Nos.	Conventional 2-level Inverter	Multilevel Inverter
1.	Square wave output voltage.	Stair-case wave output voltage.
2.	Higher THD in output voltage.	Low THD in output voltage.
3.	High voltage levels are not possible.	High voltage levels are possible.
4.	Not applicable for High Voltage applications.	Applicable for High Voltage applications.
5.	More switching stresses on devices.	Reduced switching stresses on devices.
6.	Since dv/dt is high the EMI from system is high.	Since dv/dt is low the EMI from system is low.
7.	Higher switching frequency is used hence switching losses are high.	Low switching frequency can be used and hence reduction in switching losses.
8.	Power bus station control schemes are simple.	Control scheme becomes complex as number of levels increases.

Basic Multilevel Inverters:

A. ***Single-phase two-level inverter:*** Consider a basic single-phase two-level inverter with its load voltage waveform shown in Fig.1.1. for explaining the operation. When switches S_1 and S_2 are closed, then the load current flows from dc source, through switch S_1, load terminals '*a*' to '*b*', switch S_2, and back to the other terminal of dc source. The load current is positive when enters into load at terminal '*a*', and the positive voltage waveform is obtained across the load. Similarly, a negative voltage waveform across the load is obtained when conduction takes place from dc source, through switch S_3, load terminals '*b*' to '*a*', switch S_4, back to another terminal of dc source. The load current is negative when enters into load terminal '*b*'. Thus, a complete load voltage waveform (Phase) is obtained as shown in Fig. 1.1 (b) and load current wave shape depends on the type of load. The load phase voltage $V_o = V_{ab}$ obtained is of two-level, appears as $+V_{dc}$ and $-V_{dc}$.

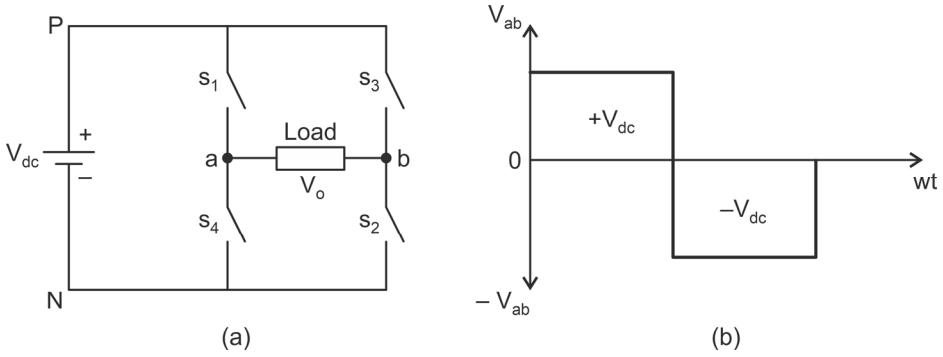


Fig. 1.1 Single-phase two-level inverter (a) Basic Circuit, (b) Load voltage waveform.

B. Three-phase two-level inverter: Now, a three-phase two-level inverter with three-phase wye-connected load is considered as shown in Fig.1.2 to represent various load voltages normally come across in the multilevel inverters and their voltage waveform varies accordingly, as the levels are increased.

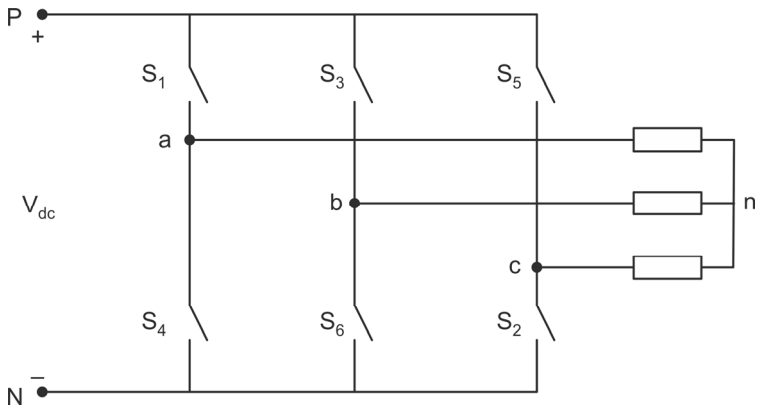


Fig. 1.2 Three-phase two-level inverter.

V_{aN}, V_{bN}, and V_{cN} are known as Pole voltages across load terminal and neutral point of the inverter circuit or second terminal of dc source 'N', respectively.

V_{an}, V_{bn}, and V_{cn} are known as Phase voltages across respective load terminal and neutral point of three-phase load 'n'.

V_{ab}, V_{bc}, and V_{ca} are known as Line voltages between phases of three-phase loads.

The typical various load voltage waveforms are shown in Fig. 1.5. – Fig. 1.7 for three level, five-level and seven-level outputs at a later-stage.

Three-phase inverter operation is explained with single-leg arrangement for easy understanding, with its load voltage waveform representing three-level output as shown in Fig. 1.3 (a) and (b). The inverter operation is explained as follows:

The inverter circuit consists of three-terminal dc sources, from which two-identical dc sources of value each V_{dc} are connected to terminals 'P' and 'N' and these terminals are separated by a mid-point terminal '*o*' and the load is connected between terminals '*a*' and '*o*'. The controlled power semiconductor switch 'S_w' is to be connected to three points of dc source terminals '1, '*o*', '2' each time and accordingly load voltage waveform varies. As the switch 'S_w' of the load terminal '*a*', when connects to the dc source terminal '1', then it produces a positive load voltage of $V_{ao} = +V_{dc}$, and similarly, when switch 'S_w' connects to the mid-point dc source terminal, then a zero load voltage appears as $V_{ao} = 0$. Finally, the switch 'S_w' when connects to dc source terminal '2', then it produces a negative load voltage, $V_{ao} = -V_{dc}$. The resultant load voltage waveform for V_{ao} is shown in Fig. 1.3 (b). Similarly, single-phase and three-phase bridge circuit topologies can be developed by adding one more leg and two more legs, respectively.

Observe the difference of load waveforms between two-level inverter and three-level inverter outputs, so that reader can easily identify the load voltage waveforms when they appear for various levels of inverters in various chapters of this book.

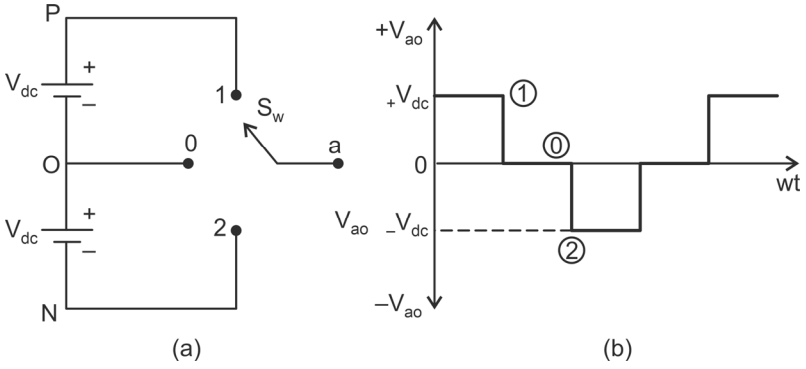


Fig. 1.3 Three-level Inverter (a) with single-leg and mid-point arrangements, and (b) three-level output voltage waveform.

From the Fig.1.3, it is noticed that the dc source voltage of the circuit is divided into two equal dc sources of each V_{dc}, separated by connecting mid-point common terminal as 'O'. Then the resultant three-level output voltage waveform is also divided into two parts, one representing positive and another representing negative separated by zero-period. In order

to judge the three-level output voltage between load terminal '*a*' and mid-point common terminal 'O' as V_{aO}, in such a case, one has to count the waveform from positive (1) to negative (2) including zero-period (O), thus, get the three-level output voltage waveform by counting 1, O, and 2 waves together in Fig.1.3 (b).

C. Single-phase three-level bridge inverter: Consider a single-phase bridge circuit inverter for three-level output voltage waveform as shown in Fig.1.4 (a) and (b) respectively, for the explanation of the detailed operation. The circuit topology is having two dc sources as V_1 and V_2 with three source terminals indicated as 1, 2 and 3. Two switches are provided in the circuit as S_{wa} and S_{wb} connecting the load terminals '*a*' and '*b*' to three source terminals one at a time in proper sequence, respectively, in order to obtain a regular three-level output voltage (V_{ab}) waveform. Switch S_{wa} can be connected to dc source terminals 1, 2 and 3 to obtain positive output voltage across the load as $V_1 + V_2$, either V_1 or V_2 and zero voltage respectively. Similarly Switch S_{wb} can be connected to dc source terminals 3', 2' and 1' to obtain negative output voltage across the load as zero voltage, either V_1 or V_2 and $V_1 + V_2$, respectively.

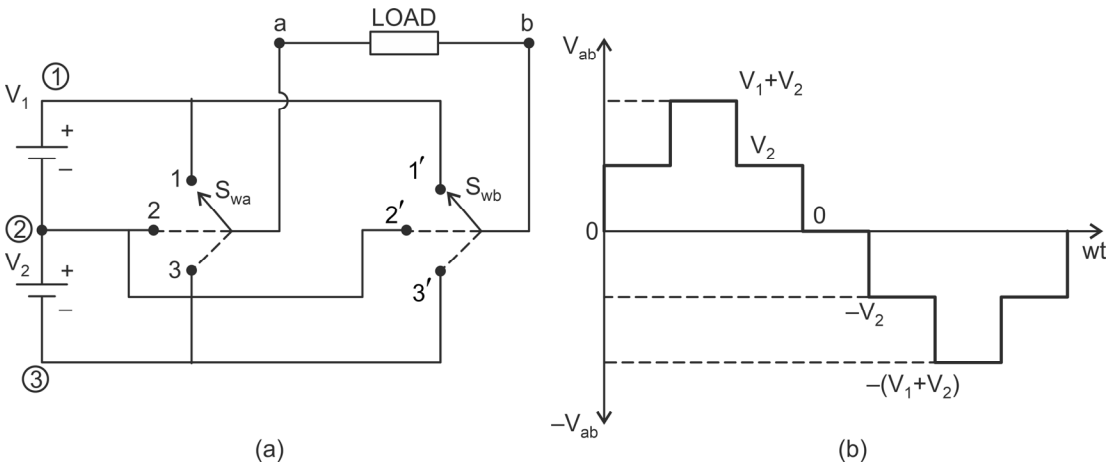


Fig. 1.4 Single-phase three-level bridge inverter (a) Basic single-phase bridge circuit inverter, (b) three-level output voltage (V_{ab}) waveform.

The operation of the above circuit topology is presented in six modes as follows and the switching sequence and respective output voltages are given in table 1.1.

Mode 1: To obtain $V_{ab} = + (V_1+V_2)$, the switch S_{wa} is to be connected to dc source terminal 1 and switch S_{wb} is to be connected to dc source terminal 3', respectively, and load current I_a flows from load terminals '*a*' to '*b*' is considered as positive current.

Mode 2: To obtain $V_{ab} = +V_2$, the switch S_{wa} is to be connected to dc source terminal 2 and switch S_{wb} is to be connected to dc source terminal 3', respectively, and load current I_a flows from load terminals '*a*' to '*b*' is considered as positive current.

Mode 3: To obtain $V_{ab} = 0$, the switch S_{wa} is to be connected to dc source terminal 3 and

switch S_{wb} is to be connected to dc source terminal 3', respectively, and load current I_a is zero.

OR

Mode 4: To obtain $V_{ab} = 0$, the switch S_{wa} is to be connected to dc source terminal 1 and switch S_{wb} is to be connected to dc source terminal 1', respectively, and load current I_a is zero.

Mode 5: To obtain $V_{ab} = -V_2$, the switch S_{wa} is to be connected to dc source terminal 3 and switch S_{wb} is to be connected to dc source terminal 2', respectively, and load current I_a flows from load terminals '*b*' to '*a*' is considered as negative current.

Mode 6: To obtain $V_{ab} = -(V_1+V_2)$, the switch S_{wa} is to be connected to dc source terminal 3 and switch S_{wb} is to be connected to dc source terminal 1', respectively, and load current I_a flows from load terminals '*b*' to '*a*' is considered as negative current.

Table 1.2 Switching sequence and output voltages.

Modes	Switch S_{wa}	Switch S_{wb}	Output Voltage, V_{ab}	Load current, I_a
Mode 1	Terminal -1	Terminal -3'	+ (V_1 + V_2)	Positive
Mode 2	Terminal -2	Terminal -3'	+ V_2	Positive
Mode 3	Terminal -3	Terminal -3'	Zero Voltage	Zero
Mode 4	Terminal -1	Terminal -1'	Zero Voltage	Zero
Mode 5	Terminal -3	Terminal -2'	- V_2	Negative
Mode 6	Terminal -3	Terminal -1'	- (V_1 + V_2)	Negative

It is observed from the Fig.1.4 that, the dc source voltages V_1 and V_2 are not divided as it was done in Fig.1.3, and the output voltage in this case is measured between load terminals '*a*' and '*b*', unlike in Fig.1.3 where output voltage is measured between load terminal '*a*' and common mid-point terminal 'O'. The resultant output voltage is counted from only positive side of the waveform, for three-level, it is counted as $+(V_1+V_2)$, $+V_2$ and 0 together, but not counted both positive and negative sides of the waveform, if counted so, it will lead to five-level waveform, which is not correct.

Now it is appropriate to present various type of output voltages for three-phase bridge inverter shown in Fig.1.2 earlier for three-level. If the same three-phase bridge inverter is developed for five-level and seven-level and their typical (i) Line to mid-point Voltage, (Pole Voltage),V_{ao} (ii) Line to line Voltage, V_{ab} and (iii) Phase to neutral of star-connected load Voltage waveforms, (Phase Voltage) V_{an} are given in Fig. 1.5 (a), (b), (c) for three-level voltages and in Fig. 1.6 (a), (b), (c) for five-level voltages and Fig. 1.7 (a), (b), (c) for seven-level voltages, respectively, to observe the difference in representing various voltage waveforms and their respective waveshapes for better understanding and clarity.

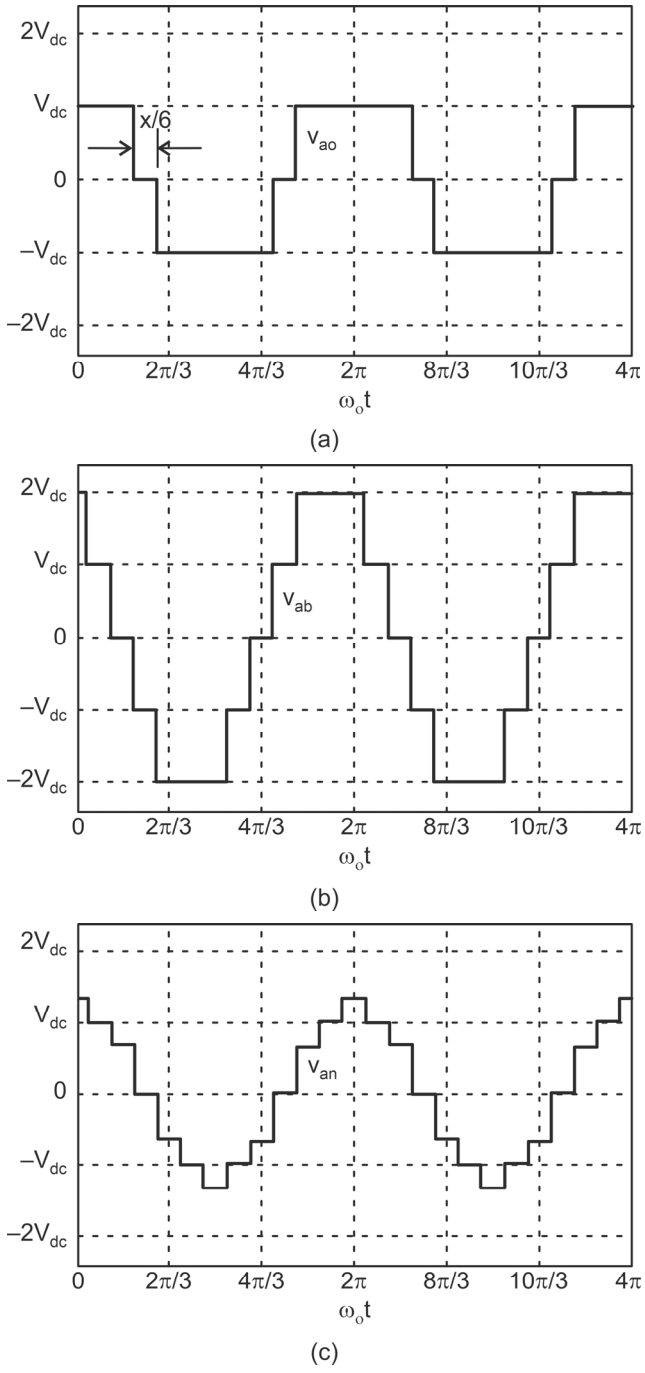


Fig. 1.5 Three-phase Three-level Inverter, typical (a) Pole Voltage, (line-to-midpoint), V_{ao}, (b) Line-to-line Voltage, V_{ab} and (c) line-to-neutral Voltage, V_{an}, (Phase Voltage) waveforms.

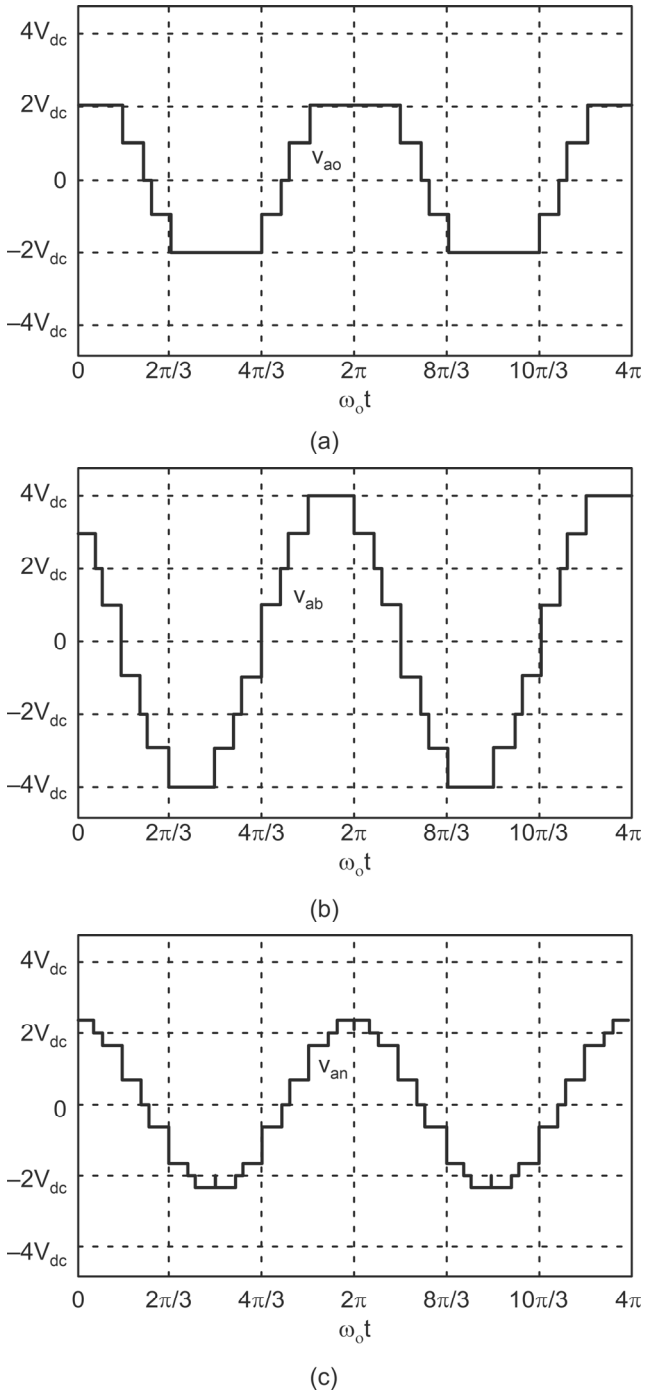


Fig. 1.6 Three-phase Five-level Inverter, typical (a) Pole Voltage, (line-to-midpoint), V_{ao}, (b) Line-to-line Voltage, V_{ab} and (c) line-to-neutral Voltage, V_{an}, (Phase Voltage) waveforms.

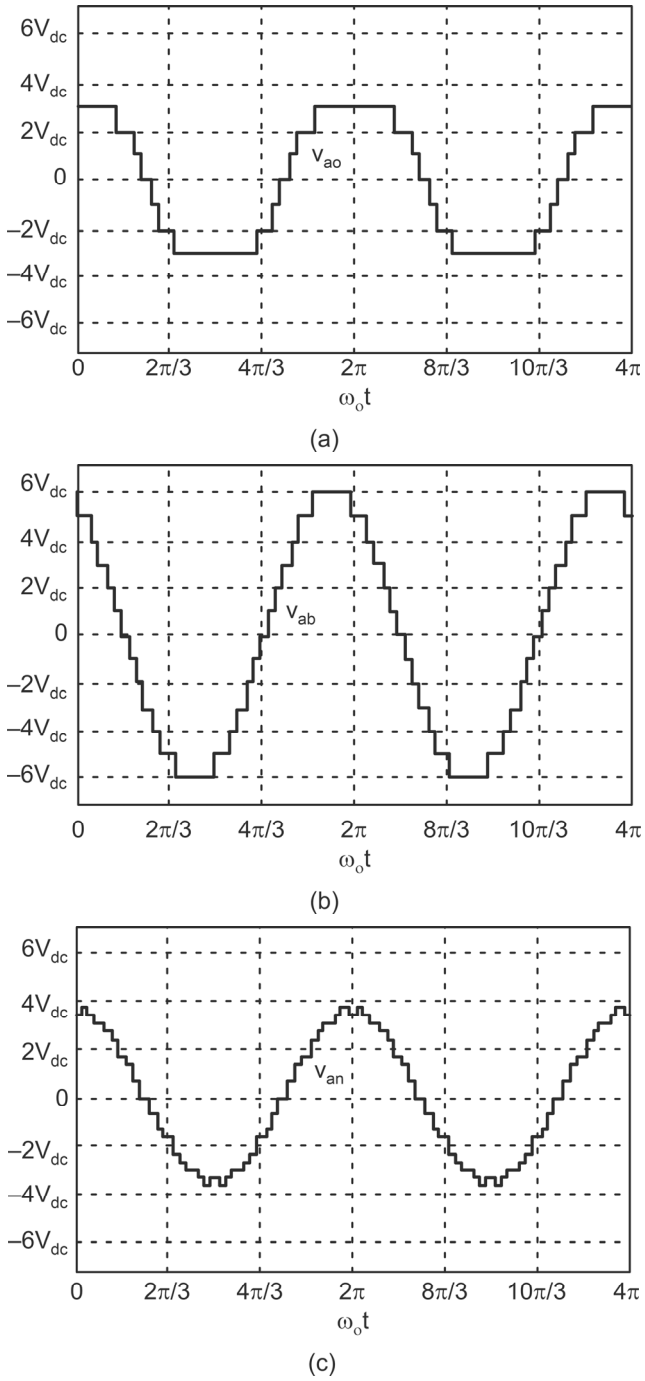


Fig. 1.7 Three-phase seven-level Inverter, typical (a) Pole Voltage, (line-to-midpoint), V_{ao}, (b) Line-to-line Voltage, V_{ab} and (c) line-to-neutral Voltage, V_{an}, (Phase Voltage) waveforms.

D. m-level generalized inverter: The m-level generalized inverter circuit is shown in Fig. 1.8, where the load terminal 'O' is connected through switch to various dc source terminals from V_1 to V_m. The output voltage V_o can be varied from V_1, V_2, . . ., $V_m/2$, $V_m/2$ -1, . . ., V_m -1, and V_m.

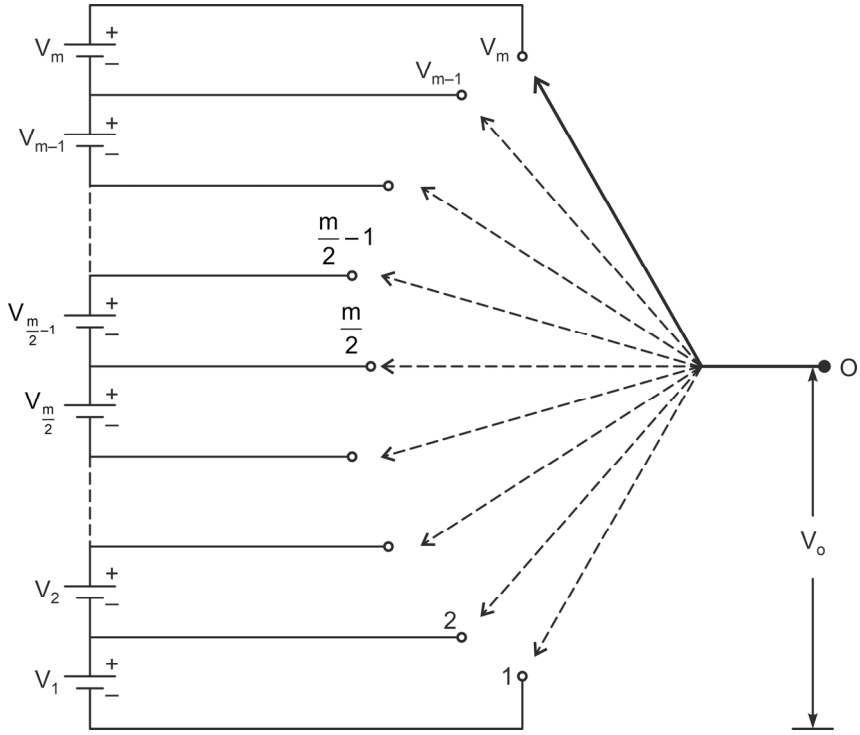


Fig. 1.8 m-level inverter.

1.2 Classification of Multilevel Inverters

The multilevel inverters are classified in various topologies based on voltage clamping facilities. They are

1. Diode-clamped multilevel inverters
2. Flying capacitor multilevel inverters
3. Cascaded H-bridge inverters
4. Hybrid Multilevel inverters

1. **Diode-clamped multilevel inverters:** In diode-clamped multilevel inverters the diodes are used as the clamping devices to clamp the d.c. bus voltage so as to achieve steps in the output voltage. It requires more clamping diodes.
2. **Flying capacitor multilevel inverters:** In flying capacitor multilevel inverters, the flying-capacitors are used to clamp the d.c. bus voltages to achieve steps in the output voltage. It requires more clamping capacitors.

3. **Cascade H-bridge inverters:** Several units of single phase full bridge inverters with separate d.c. source is connected in series to increase the number of levels in output voltage and acts as cascaded H-bridge multilevel inverters. Clamping diodes and clamping capacitors are not required.
4. **Hybrid Multilevel Inverters:** Hybrid topologives are also recently developed for making the quality of output voltage waveforms to which it requires higher number of different voltage magnitude dc sources. Generally, asymmetric dc source multilevel inverters generate higher output voltage steps with lower percentage of asymmetric. Total harmonic distortion compared with symmetric dc source multilevel inverters.

They can be used for single-phase, three-phase, five-phase and six-phase inverters of all the above three varieties. The multilevel inverters start from two-level, three-level, four-level, five-level, continues up to m-level inverters. The diode-clamped three-level inverters are popularly known as Neutral Point Clamped (NPC) inverters. Diode-clamped multilevel inverters or NPC inverters are presented in the chapter:3, in chapter:4, Flying capacitor multilevel inverters are discussed, Cascaded H-bridge inverters are explained in chapter:5, and in chapter:6 Hybrid multilevel inverters. The constructional details, basic operations, various levels, various topologies, advantages, disadvantages and applications are presented for all the four classified topologies.

1.3 Harmonic Distortions

Introduction: The basic two-level inverter can generate a square-wave output ac voltage of various frequencies across the load. The square-wave voltage consists of harmonic components of multiple frequencies, but the load demands pure sinusoidal waveform with zero harmonic component. The multilevel inverters also generate a non-sinusoidal voltage waveform and current waveform. When waveforms deviate from a sinewave shape, they contain harmonics. These current harmonics distort the voltage waveform and create distortion in the power system which can cause many problems. A power system can contain one or two different kinds of loads, a non-linear load or a linear load. Non-linear loads such as adjustable speed drives, power supplies for various electronic equipment are the origin of both current and voltage harmonics production in the distribution system leading to the power quality problem. In response to the power quality problem, IEEE 519 and IEC EN 61000-3 standards specify regulations governing harmonic compliance.

Some of the effects the harmonic can cause, to the equipment, to the installation, or both, are:

- Electronic equipment may be sensitive to the voltage distortion supplying it, due to higher voltage peaks, unexpected zero-crossing, affectation to protection circuits, etc.
- Digital circuits can be affected by misinterpretation of logical values in presence of harmonics.
- Reduced service life of components and equipment under continuous distorted supply voltage.
- Affectation of IT equipment such as memory losses, and turn offs.

- Uninterruptible Power Supplies may need to handle with high distorting loads, i.e., high current peaks may be over the range of the crest factor capacity of this UPS. In such case, the voltage distortion can even increase, if the inverter of the UPS is not capable enough.
- Added efficiency losses to the system composed by electrical installation and equipment.
- Unexpected resonances.
- Unwanted overload (or need to oversize) for transformers, and wirings.
- Malfunctions of motors and generators.
- Unwanted Circuit Breakers tripping or Fuses blowing.

As per the standards, IEEE 519: Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, individual harmonic limit is 5%, Total harmonic distortion for low voltage is 8%. Some of the higher-order harmonics can be filtered out by using passive and active harmonic filters.

1.4 Classification of Modulation Techniques

The multilevel inverters are employed for facilitating variable output voltages at various frequencies or fixed frequency for a load or for a power system from a fixed dc source. The variation in output voltage is possible within the inverter by applying a suitable modulation technique for controlling the switching pattern of the inverter.

Pulse width modulation is a great method of controlling the amount of power delivered to a load without dissipating any wasted power. The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is almost no voltage drop across the switch.

Applications of Pulse Width Modulation (PWM): Techniques reduces the overall harmonic distortion THD in a load current.

- Pulse Width Modulation helps in voltage regulation and thus finds its use in controlling the speed of motors.

Advantages of Pulse Width Modulation (PWM): The advantages are:

- Pulse Width Modulation provides accuracy and quick response time.
- It provides high input Power Factor.
- Initial cost is low.
- PWM technique helps the motors to generate maximum torque even when they are running at lower speeds.

Disadvantages of Pulse Width Modulation (PWM): The disadvantages are:

- As the PWM frequency is high, switching losses is considerably high.
- It induces Radio Frequency Interference (RFI).

The modulation techniques are classified as follows:

1. Pulse width modulation (PWM) techniques:
   - Sinusoidal Pulse width modulation (SPWM) scheme.
   - Third Harmonic Injected Pulse width modulation (THI-PWM) scheme.
   - Selective Harmonic Elimination Pulse width modulation (SHE-PWM) scheme.
2. Carrier based pulse width modulation (CB-PWM) techniques:
   - Phase-shifted Carrier-based pulse width modulation (PS-CB-PWM) scheme.
   - Level-shifted Carrier-based pulse width modulation (LS-CB-PWM) schemes.
     - Phase Disposition carrier-based pulse width modulation (PD-CB-PWM) method.
     - Phase Opposition Disposition carrier-based pulse width modulation (POD-CB-PWM) method.
     - Alternate Phase Opposition Disposition carrier-based pulse width modulation (APOD-CB-PWM) method.
3. Space Vector modulation techniques:
   - Two-dimensional (2-D) algorithm scheme.
   - Three-dimensional (3-D) algorithm scheme.
   - Space vector carrier-based pulse width modulation (SV-CB-PWM) scheme.

The above all pulse width modulation techniques are addressed elaborately in chapter 2.

1.5 Classification of Power Semiconductor Switching Devices

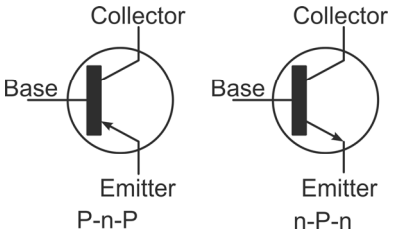
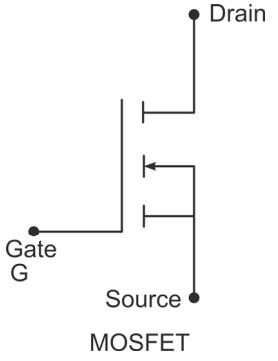
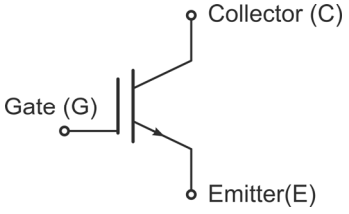
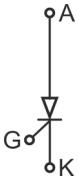
The power semiconductor switching devices play an important role in controlling the magnitude and quality of the output voltage and load current, in coordination with various pulse width modulation schemes for multilevel inverters. There are wide variety of power semiconductor switching devices available in the literature and in the market. The selection of type of power semiconductor devices depends on various factors, such as, voltage and current ratings, power handling capability, thermal ratings, switching frequencies, turn-on and turn-off times, conduction and switching losses, voltage blocking capabilities, safe operating area (SOA), etc.

The classification of power semiconductor switching devices are given as follows.

1. Transistor Family Devices:
   - Power Bipolar Junction Transistor (BJT) devices.
   - Power MOSFET (Metal-Oxide Field-effect transisitor) devices.
   - Power IGBT (Insulated Gate Bipolar Transistor) devices.
2. Thyristor Family Devices:
   - Thyristor Power Devices.
   - Gate Turn-Off (GTO)-Thyristor Power Devices.

3. Transistor-Thyristor Family Devices:
   - Power IGCT (Insulated Gate Commutated Thyristor) Devices.
   - Power ETO (Emitter Turn-Off) Thyristor Devices.
   - Power MTO (MOS Turn-Off) Thyristor Devices.
   - Power MCT (MOS Controlled Thyristor) Devices.
   - Static Induction Thyristor (SITH) Devices.

Table. 1.3 Various Power Semiconductor Switching Devices and their symbols.

Sl.no.	Name of the Device	Symbols
1.	Transistor Family Devices	
1.1	BJT (Bipolar Junction Transistor)	
1.2	MOSFET (Metal-Oxide Semiconductor Field Effect Transistor)	
1.3	IGBT (Insulated Gate Bipolar Transistor)	
2.	Thyristor Family Devices	
2.1	Thyristor	

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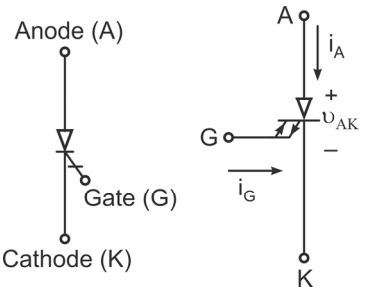
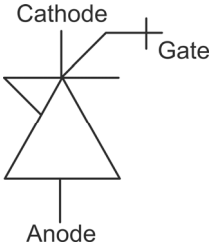
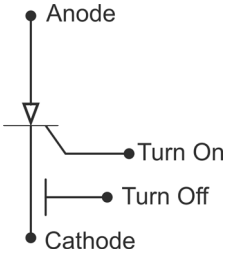
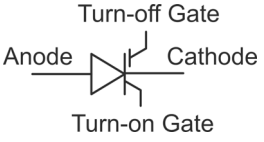
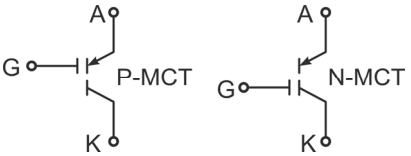
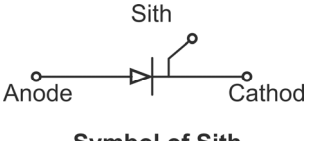
Sl.no.	Name of the Device	Symbols
2.2	GTO-Thyristor (Gate-Turn-Off-Thyristor)	
3.	Transistor-Thyristor Family Devices	
3.1	IGCT (Insulated Gate Commutated Transistor)	
3.2	ETO – Thyristor (Emitter Turn-Off -Thyristor)	
3.3	MTO – Thyristor (MOS-Turn-Off – Thyristor)	
3.4	MCT – Thyristor (MOS-Controlled-Thyristor)	
3.5	SITH – Thyristor (Static-Induction Thyristor)	 **Symbol of Sith**

1.6 Applications of Multilevel Inverters

The Multilevel Inverters are used in industrial motor drives, hybrid electric vehicles, locomotives drives, AC power transmission systems (FACTS) such as STATCOMs, SSSC, UPFC, AC distribution systems (PQ) such as DVR, D-STATCOM, UPQC, HVDC Transmission Systems such as converter and inverter stations, Standby power supplies and custom power devices, etc.

1.7 Summary

This chapter deals with the brief introduction of Multilevel inverters, their importance, basic circuits and operations, typical output voltage waveforms. The importance of Pulse width modulation for multilevel inverters and their classifications are also presented for clarity. The availability and suitability of power semiconductor switching devices along with their symbols are given for ready reference. The multilevel inverters are having advantages of producing 15% more output voltage with less harmonics by synthesizing compared to their conventional multi-pulse inverters. In recent years, the multilevel inverters are very widely used in many applications in the area of industrial drives, power transmission and distribution, and renewable energy systems.

Learning Outcomes

- To be able to acquire knowledge about importance of Multilevel inverters and to be able to give classification of various multilevel inverters. (CO1) :: (PO1)
- To be able to acquire knowledge about importance of pulse width modulation techniques and to be able to give classification of various schemes of pulse width modulations. (CO1):: (PO1)
- To be able to understand the power semiconductor devices, their symbols and names of the terminals and application of suitable device to multilevel inverters. (CO2) :: (PO1)

Questions

1.1 Classify multilevel inverters?
1.2 Discuss the features of multilevel inverter over conventional two-level inverter?
1.3 Explain the operation of basic single-phase two-level inverter with its output voltage?
1.4 Explain the operation of basic three-level inverter with single-leg arrangement and its output voltage?
1.5 Discuss the working of basic single phase three-level bridge inverter with its output voltage with the help of various modes?
1.6 Draw the pole voltage (line-to-midpoint), phase voltage (line-to-neutral), and line voltage(line-to-line) waveforms for three-phase three-level inverter?
1.7 Draw the pole voltage (line-to-midpoint), phase voltage (line-to-neutral), and line voltage(line-to-line) waveforms for three-phase Five-level inverter?
1.8 Draw and explain m-level generalized inverter basic diagram?

1.9 Discuss the effects of harmonics on the performance of the electrical equipment and installations?
1.10 Give advantages and disadvantages of pule width modulation?
1.11 Classify Sinusoidal Pulse width modulation techniques?
1.12 Classify Carrier based Pulse width modulation techniques?
1.13 Classify Space Vector Modulation techniques?
1.14 Name various power semiconductor devices?
1.15 Give applications of multilevel inverters?
1.16 Draw the symbols of Power BJT and Power IGBT with the name of the Terminals?
1.17 Draw the symbol of Power MOSFET with the name of the Terminals?
1.18 Draw the symbols of Power Thyristor and GTO-Thyristor with the name of the Terminals?
1.19 Draw the symbol of Power IGCT with the names of the terminals?
1.20 Draw the symbols of Power ETO, MTO and MCT with the names of the terminals?

Multiple Choice Questions

1.1 Identify the terminals of the power Bipolar Junction Transistor (BJT),
(a) Collector, Anode, Cathode (b) Emitter, Collector, Base
(c) Anode, Emitter, Base (d) Cathode, Collector, Emitter

1.2 Choose the appropriate terminals of the power IGBT
(a) Collector, Emitter, Base (b) Cathode, Anode, Gate
(c) Collector, Emitter, Gate (d) Collector, Anode, Base

1.3 Identify the terminals of the power MOSFET
(a) Anode, Cathode, Gate (b) Collector, Emitter, Base
(c) Source, Drain, Base (d) Source, Drain, Gate

1.4 Choose the appropriate terminals of the power Thyristor
(a) Anode, Collector, Gate (b) Anode, Cathode, Gate
(c) Emitter, Collector, Base (d) Gate, Anode, Emitter

1.5 Identify the terminals of the power GTO-Thyristor
(a) Cathode, Emitter, Gate
(b) Collector, Base, Cathode
(c) Anode, Cathode, bidirectional Gate
(d) Emitter, Base, Anode

1.6 Choose the appropriate terminals of the power IGCT
(a) Cathode, Anode, isolated Gate
(b) Cathode, Anode, bidirectional Gate
(c) Cathode, Anode, Base
(d) Collector, Emitter, Base

1.7 Identify the terminals of the power ETO
(a) Anode, Cathode, Turn-on Gate, Turn-off Gate
(b) Gate, Anode, Cathode
(c) Base, Collector, Emitter
(d) Collector, Cathode, Gate

1.8 Choose the appropriate terminals of the power MTO
(a) Anode, Cathode, Gate1 for Turn-on, Gate2 for Turn-off
(b) Base, Collector, Anode
(c) Gate for turn-on, Gate for turn-off, Emitter, Collector
(d) Anode, Cathode, Base for turn-on, Base for turn-off

1.9 Identify the terminals of the power MCT
(a) Anode, Cathode, connected Gate
(b) Anode, Cathode, Base
(c) Anode, Cathode, isolated Gate
(d) Collector, Emitter, Base

1.10 Choose the appropriate terminals of power SITH
(a) Anode, Cathode, Base (b) Anode, Cathode, Gate
(c) Emitter, collector, Base (d) Emitter, Collector, Gate

1.11 How many schemes of sinusoidal pulse width modulation for multilevel inverter are presented in this chapter
(a) three (b) two
(c) one (d) none

1.12 How many schemes of carrier-based pulse width modulation for multilevel inverters are discussed in this chapter
(a) one (b) two
(c) three (d) four

1.13 How many methods of level-shifted pulse width modulation for multilevel inverters are Presented
(a) one (b) two
(c) four (d) three

1.14 How many Space Vector Modulation schemes are available for multilevel inverters
(a) three (b) two
(c) one (d) none

Answers to Multiple Choice Questions

1.1	(b)	1.2	(c)	1.3	(d)	1.4	(b)	1.5	(c)
1.6	(b)	1.7	(a)	1.8	(a)	1.9	(c)	1.10	(b)
1.11	(a)	1.12	(b)	1.13	(d)	1.14	(a)		