Ultra-Low Noise MEMS Accelerometer Interface Circuit for Robotic Localization and Control applications

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***Abstract*— This work presents the design and evaluation of a high-resolution, single-axis MEMS accelerometer interface employing a chopper-stabilized capacitance-to-voltage converter (CVC) optimized for ultra-low noise and wide dynamic range applications. The circuits have been, implemented in the 350 nm CMOS process with a 5 V supply. The proposed circuit achieves a total-noise-equivalent acceleration (TNEA) of less than 0.57 mg/√Hz over a 200 Hz signal bandwidth with a second-order low-pass filter, surpassing conventional CVC implementations by an order of magnitude. The system demonstrates a capacitance-to-acceleration sensitivity of 7 fF/g (for nominal capacitance of 1.8 pF), voltage-to-capacitance sensitivity of 15mV/fF and a voltage sensitivity of 105 mV/g, yielding a full-scale linear response up to 30 g. Offset correction capability of 210 fF ensures robust operation against parasitic variations, while the sensing resolution of 50 aF guarantees fine detection of sub-milligravity signals. The chopper stabilization technique effectively suppresses 1/f noise and offset drift, enabling a signal-to-noise ratio (SNR) of 10 under low-g input conditions and maintaining high fidelity across the measurement range. Comparative analysis confirms that the achieved input-referred noise floor <60uV/√Hz positions this design as superior to state-of-the-art general-purpose and low-noise CVC architectures, where typical TNEA values exceed several milligravities. The resulting interface circuit provides a scalable, power-efficient(2mW) solution for precision inertial sensing, paving the way for next-generation navigation, structural monitoring, and robotic applications.**

Keywords*— *MEMS accelerometer, capacitance-to-voltage conversion, chopper stabilization, offset correction, CMOS

I. INTRODUCTION

In robotic systems, MEMS accelerometers employing capacitive-to-voltage converters(CVC) readout are pivotal for inertial sensing across both legged and wheeled platforms. For legged robots, such accelerometers support balance control and gait stabilization, particularly in wheel-legged systems where stability must be maintained under variable payload and terrain conditions [1]. In wheeled robots, these sensors form the backbone of robust dead-reckoning frameworks—especially when mounted on wheels to reduce bias drift and improve velocity estimation—and also assist in slip detection via sensor fusion [2][3].These capabilities significantly enhance navigation, stability, and autonomy, making CVC-based MEMS accelerometers particularly attractive for defence, industrial, and exploration applications.

While MEMS accelerometers offer advantages such as compact size and low power consumption, their readout circuits are often constrained by low-frequency noise, capacitive offset drift, and signal integrity limitations [16]. Chopper stabilization mitigates 1/f noise and to some extent the operational transconductance amplifier-OTA offset problems, but robotic deployment further requires programmable bandwidth, shock handling, and full range analog interfacing. This work presents a readout system tailored for these needs. For high-g range sensing (e.g., up to 30g), accurate signal conditioning is essential to convert minute capacitive variations into measurable voltages. However, thermal noise, offset drift, and OTA (CMOS) nonlinearity, mismatch of capacitance, inaccuracies in CMOS process limit the performance of conventional readout circuits.

Chopper stabilization has emerged as a robust technique to suppress low-frequency noise in CMOS front-end amplifiers [6]. In this work, we present a chopper-stabilized C-V (section 2) converter with an integrated offset correction circuit tailored for a 30g MEMS accelerometer. The design is implemented (section 3, 4 & 5) in a 350 nm CMOS technology, providing a balance between voltage headroom, analog performance, and cost. The test results (Section 6) are in line with specifications required for robotic applications. Achieved results are compared in section 7 and paper is concluded in section 8.

II. SYSTEM OVERVIEW

A. Architecture

The MEMS accelerometer consists of a fixed structure and a movable proof mass forming a differential capacitive bridge. The capacitance change (ΔC) is proportional to the applied acceleration. This architecture translates the tiny capacitance variations (tens of fF per g) into a rail-to-rail voltage output suitable for downstream digital conversion. Block Diagram of CVC circuits is shown in follows figure:

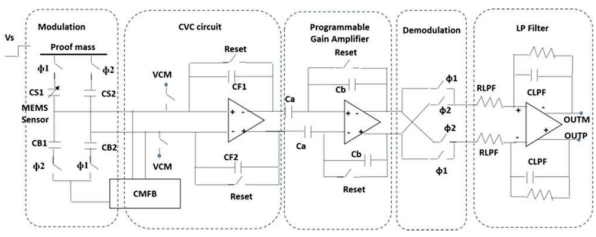


Figure 1: Architecture of CVC

The complete switched-capacitor interface circuit, illustrated in Figure 1, integrates the MEMS sensor, a capacitance-to-voltage converter (CVC), a variable-gain amplifier (VGA), synchronous demodulator, and low-pass filter (LPF) into a unified signal chain optimized for high-resolution inertial sensing. The MEMS sensor operates as a differential capacitive transducer, where the capacitance variation (ΔC) due to proof-mass displacement is proportional to applied acceleration. This differential capacitance is modulated through a chopping clock, up-converting low-frequency sensor signals and effectively suppressing flicker noise. The CVC stage utilizes switched-capacitor techniques with accurately matched capacitor banks and bias-controlled switches to convert the modulated signal charge into a differential voltage, ensuring high linearity and minimal offset. The VGA, also realized with switch enabled variable capacitor gain control, provides tuneable amplification across varying input signal conditions, ensuring compatibility with incoming modulated signal. Following amplification, the synchronous demodulator, driven by the same non-overlapping clock phases, recovers the baseband acceleration signal by coherently demodulating the chopped carrier. Finally, a Sallen-Key [7]low-pass filter attenuates residual chopping ripple and harmonics, yielding a clean, low-noise output voltage. With a chopping frequency of 25 kHz and a dynamic range (DR) of 81 dB, this architecture achieves excellent noise suppression, programmability, and robustness, making it highly suitable for precision MEMS accelerometer readout in navigation and robotic applications.

B. MEMS Accelerometer Specifications

Overall specifications required for MEMS Accelerometer along with CVC readout circuit are given in Table 1.

Table 1: Overall Specifications

Category	Specification
Measurement Range	0-30 g
Linearity Error	< 0.1% Full Scale (FS)
Noise Performance	TNEA < 0.57 mg/√Hz
Resolution	~50 aF
Signal-to-Noise Ratio	10
Sensitivity	105 mV/g
Nominal Capacitance	1.8 pF
Signal Bandwidth	200 Hz
Offset Correction	Up to 210 fF
Residual Offset (Trimmed)	< 1 mg
Filtering	2nd-Order Low Pass Filter
Supply Voltage	5 V
Power Consumption	< 2 mW

III. CIRCUIT DESIGN

A. Chopper Modulated CVC

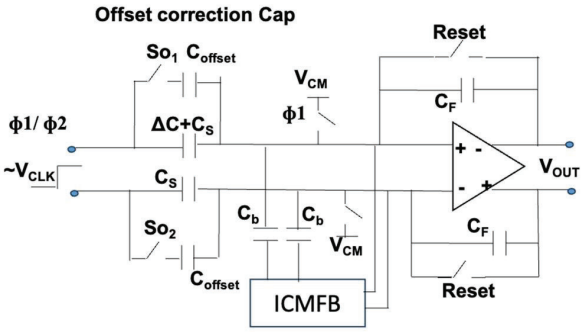


Figure 2: CVC circuit interface with accelerometer

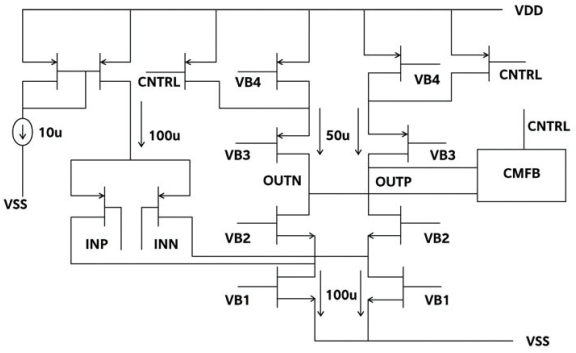
In this work, the folded cascode OTA was employed in a closed-loop chopper-stabilized [7] capacitive-to-voltage converter (CVC) for MEMS accelerometer readout applications. The accelerometer under test exhibits a base capacitance of 1.8 pF, and the chopper modulation frequency was set to 25 kHz to effectively up-convert low-frequency flicker noise and offset, thereby improving signal fidelity.
The input capacitive bridge was realized using a tunable capacitor bank (Cs±ΔC) for differential sensing of capacitance variations, while the bias capacitors (C_b) and feedback capacitors (C_f) ensured proper charge transfer and closed-loop linearity. High-value poly-resistors were used to define the low-frequency cutoff without occupying excessive silicon area. An input common-mode feedback (ICMFB) block (Figure 2) was incorporated to stabilize the common-mode output voltage of the OTA under varying input conditions. A reset mechanism was also incorporated across the feedback capacitance of CVC to discharge the C_f regularly. The resulting CVC achieves low noise, high linearity, and wide dynamic range, making it suitable for precision low-frequency acceleration sensing over signal bandwidth of 200 Hz.

B. Capacitively coupled Instrumentation Amplifier

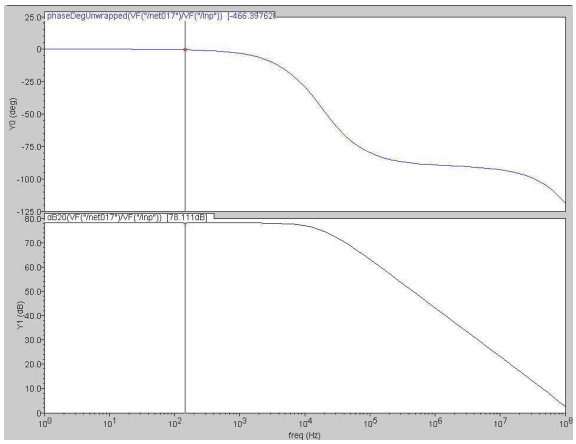
A folded cascode [10] [11] [12] [13] operational transconductance amplifier (OTA) was designed and implemented in a standard CMOS process with a supply voltage of 5V and a bias current of 100 µA. The proposed OTA (as shown in Figure 3) achieves a high open-loop DC gain of 78 dB, ensuring sufficient amplification for precision analog front-end applications.

The circuit provides a wide output voltage swing of 4 Vpp , which enhances dynamic range, while maintaining a unity gain bandwidth of 10 MHz with a phase margin of 76°, thus guaranteeing stable closed-loop operation. To improve common-mode stability, a common-mode feedback (CMFB) circuit was utilized suitably. Furthermore, the integrated output noise over the signal bandwidth of 200 Hz was limited to ≤ 2 mVrms, enabling low-noise signal processing suitable for sensor interface circuits. The combination of low power consumption, high gain, wide swing, and noise performance makes this folded cascode OTA architecture an effective

choice for low-frequency, high-precision analog signal processing applications.



(a)



(b)

Figure 3: OTA circuit (a) with CMFB, and (b) AC response

C. Programmable Gain Ampplifier:

The proposed high-gain folded cascode OTA was further utilized in the design of a programmable gain amplifier (PGA) employing a switched-capacitor capacitor bank (as shown in Figure 4) for gain programmability. The closed-loop gain of the circuit is tunable in the range of 2–15 (well-established in prior art [14], [15]) through appropriate selection of the capacitor ratios (C_{gain1}, C_{gain2}, C_f), allowing flexibility for diverse sensing conditions. A nominal closed-loop gain of 8 was chosen to achieve the required sensitivity of 15 mV/fF for the accelerometer interface, ensuring accurate translation of sub-femtofarad capacitance variations into measurable voltages. The switched-capacitor architecture not only enables precise gain control but also ensures robust linearity and low offset, making the PGA well-suited for low-frequency, high-resolution sensor front-end applications.

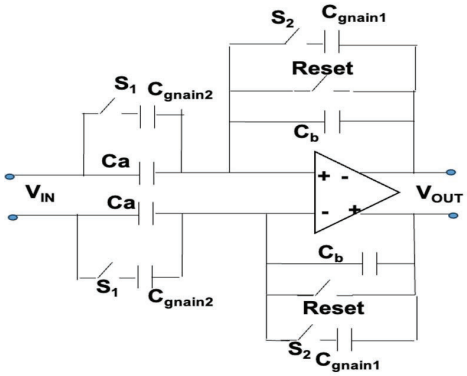


Figure 4: PGA circuit

D. Synchronous Demodulation & LPF:

A correlated demodulator and Sallen Key (SK) low-pass filter [7]recover the baseband voltage proportional to acceleration. Chopping creates ripple at and its harmonics. An active Sallen-Key LP filter senses ripple and attenuate it by >40 dB without increasing in-band noise. Synchronous demodulation using non-overlapping clocks φ1/φ2 followed by an SK LPF (2-pole at 800 Hz) recovers the baseband.

E. On-Chip References & Temperature Sensor:

A bandgap and PTAT [7]generator bias the OTA and allow temperature-aware on-chip calibration updates.

F. Clocks:

Non-overlapping clocks φ1/φ2 with 50 ns dead time operated at 25KHz has been used to cater the switched capacitor and chopper circuits. ; Suitable shielding for clock routing has been used to minimize feedthrough problems. Nonoverlapping clocks φ1 and φ2 are shown in Figure 5.

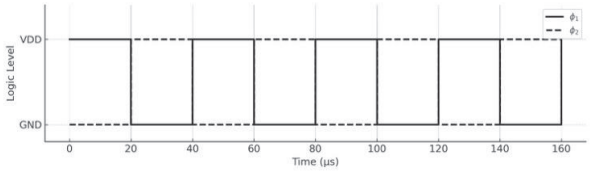


Figure 5: Non-overlapping clocks φ1/φ2

IV. NOISE, GAIN, AND SENSITIVITY ANALYSIS

Chopping operation moves input-referred 1/f noise at the out of band frequencies [4]. The baseband noise density is dominated by OTA thermal noise and kT/C at sampling capacitor, whereas flicker noise(1/f) and mismatch of capacitor dominate at hold (feedback) capacitor of the circuit. Selecting (MIM array) limits kT/C (thermal noise due to capacitor and switch resistance) to <10 μV_{rms} over 200 Hz. The clock frequency should be chosen so as to suppress the flicker noise (derived from flicker corner frequency of OTA noise response)

A. Sensitivity Chain

Capacitance-to-voltage (CVC) gain is

$$S_C = \partial V/\partial C \ (V/F) = 15 \text{ mV/fF} \quad (1)$$

$$= 15\times10^{-3} \text{ V}/10^{-15}\text{F} = 1.5\times10^{-13} \text{ V/F and}$$

While the mechanical-to-capacitance sensitivity of the accelerometer is

$$S_{C,g}=\partial C/\partial g \text{ (F/g)} = 7 \text{ fF/g} = 7\times10^{-15} \text{ F/g.} \quad (2)$$

Overall voltage-to-acceleration sensitivity is

$$S_{V,g}=\partial V/\partial g=S_C\cdot S_{C,g} \text{ (V/g)} =1.5\times1013\cdot7\times10^{-15} \quad (3)$$

$$\approx105 \text{ mV/g}$$

B. From output noise density to TNEA

$e_{n,out}$ = output-referred white noise density (V/√Hz), B = bandwidth (Hz), output rms noise voltage is

$$\sigma_v=e_{n,out}.(\sqrt{B}) \quad (4)$$

This noise can be referred back to an equivalent capacitance resolution as

$$\sigma_C=\sigma_v/S_C = \text{capacitance resolution (rms, F).} \quad (5)$$

an acceleration resolution is

$$\sigma_a=\sigma_v/S_{V,g} \text{ (rms, g)} \quad (6)$$

$$\text{TNEA} =e_{n,out}/S_{V,g} \quad (7)$$

$$\Rightarrow e_{n,out}= \text{TNEA}\cdot S_{V,g} \text{ for white-noise-dominated readout.}$$

For $e_{n,out}\approx60$ µV/√Hz and $S_{V,g}\approx 0.105$ V/g:

$$\text{TNEA} = 0.105 \,.\, 60 \text{ µV/√Hz} \approx 0.57 \text{ mg/√Hz}$$

C. Noise over 200 Hz and implied capacitance resolution

$$\sigma_V=e_{n,out} B \approx60 \text{ µV/√Hz}\cdot(\sqrt{200}) \approx0.85 \text{ mV}_{rms} \quad (8)$$

$$\sigma_C=S_C \sigma v \approx15 \text{ mV/fF } 0.85 \text{ mV} \approx56 \text{ aF} \quad (9)$$

This is consistent with the TNEA and BW measurements.

D. Acceleration resolution(over 200Hz)

$$\sigma_a= \sigma_v / S_{V,g}=0.85 \text{ mV} / 105 \text{ mV/g} \approx8.1 \text{ mg} \quad (10)$$

(Equivalently, $\sigma_a=\sigma_C/S_C$, g=56 aF/ (7 fF/g) ≈8 mg)

E. SNR for given test input

Define SNR for a sinusoid at a_{test}:

$$SNR=S_{V,g}\cdot a_{test} \text{ (rms)} /\sigma_v \quad (11)$$

For SNR≈10, corresponding atest is:

$$a_{test} \approx10 \quad \sigma_V /S_{V,g}\approx10\cdot 0.85 \text{ mV}/105 \text{ mV/g} \approx0.081 \text{ g}$$

(So SNR=10 is achieved around ~80 mg input over 200 Hz BW with the above noise.)

V. RESULTS

A. CVC Noise simulation

The measured output-noise spectral density of the closed-loop CVC (with the accelerometer connected) exhibits the expected 1/f region at low frequency and a flat wide-band floor at mid–high frequencies, as shown in Figure 6.

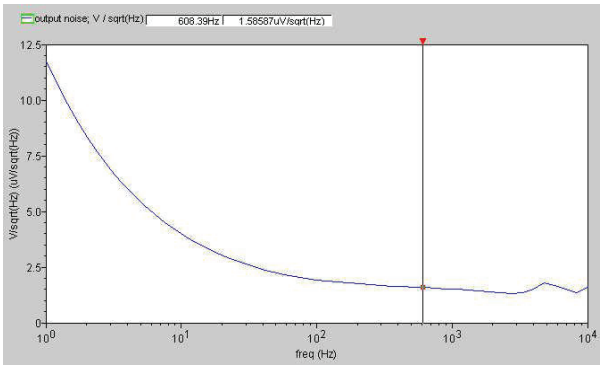


Figure 6: Output referred noise of CVC

The simulated output noise spectral density of the CVC, shown in Figure 6, demonstrates the expected trend with dominant low-frequency 1/f noise below 100 Hz, gradually transitioning to a white noise floor at higher frequencies. At low frequencies, the noise magnitude is above 10 µV/√Hz due to flicker noise contributions of the front-end amplifier and interface circuitry. As the frequency increases, the noise reduces steadily, reaching approximately 1.6 µV/√Hz around 600 Hz, and stabilizing close to 1.5 µV/√Hz beyond 1 kHz, indicating the dominance of thermal (kT/C) and bias-current noise sources. However, a noise of 60uV/√Hz @DC is observed at the input of CVC. The overall profile highlights effective suppression of low-frequency noise through circuit design and filtering, ensuring that the interface achieves a stable, low-noise performance across the operational bandwidth of the accelerometer. This characteristic makes the CVC suitable for high-resolution inertial sensing where both low offset and wide bandwidth are critical.

B. Layout Floor planning, packaging and Testing

The floorplan and layout of the fabricated ASIC were carefully optimized to achieve symmetry, noise isolation, and routing efficiency. As shown in Figure 7, the central region accommodates the capacitor array, providing matching and minimizing gradient effects across the die.

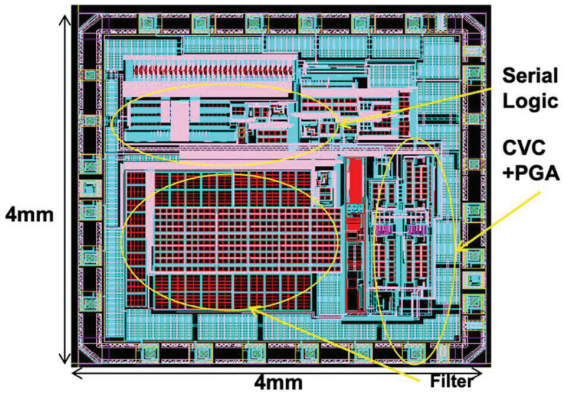


Figure 7: Floor planning and die layout

The analog signal-conditioning blocks are placed on the right side, with common-centroid placement and guard-ring structures to suppress substrate noise coupling. The biasing and reference generation circuits are located at the top, physically separated from the high-gain analog front-end to reduce interference. Peripheral I/O pads having, integrated ESD protection are kept at the boundaries surrounding the core circuit. This floor planning strategy ensures minimal parasitic coupling, improved matching for critical passive devices, and robust signal integrity, while meeting the stringent requirements of low-noise and low-power operation.

The fabricated MEMS accelerometer interface circuit was packaged in a quad flat no-lead (QFN) package with 56 pins, as shown in Figure 8. The overall package size is 8 mm × 8 mm, with a cavity dimension of 6 mm × 6 mm accommodating the silicon die. The active die area measures 4 mm × 4 mm, ensuring sufficient space for the analog front-end, biasing, and digital control blocks. Electrical interconnection between the die and package leads was implemented using 1 mil diameter gold bonding wires, chosen for their excellent conductivity, mechanical reliability, and resistance to corrosion. The short bond wire length and minimized parasitic inductance inherent to QFN package improve high-frequency performance and reduce noise coupling, which is critical in precision low-noise sensor interface circuits. Additionally, the metallic paddle on the underside of the QFN package improves thermal dissipation and provides a stable ground reference, so as to improve the signal integrity. This packaging scheme offers a compact, thermally efficient, and mechanically robust solution, suitable for integration in robotic, automotive, and aerospace sensor modules.

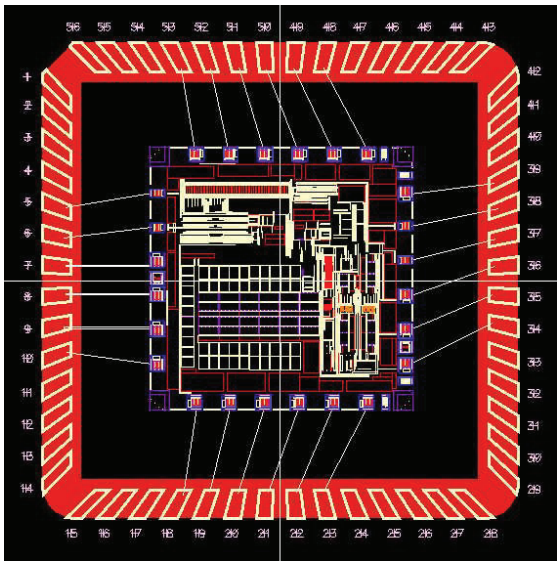


Figure 8: QFN 56 package layout with CVC die assembly

An evaluation board was developed to validate the performance of the proposed Capacitive-to-Voltage Converter (CVC) circuit in conjunction with a MEMS accelerometer. The board integrates the custom-designed CVC ASIC, highlighted in Figure. 9, with a Xilinx FPGA for digital control and data acquisition. The design also incorporates configuration switches, an interface connector, and peripheral components to enable flexible programmability and test conditions. The FPGA facilitates real-time processing and communication, while the CVC front-end provides low-noise analog readout of the sensor capacitance variations induced by external acceleration. This platform enables comprehensive characterization of the system, including noise, sensitivity, and dynamic range, under practical operating conditions, thereby establishing its suitability for high-precision inertial sensing applications.

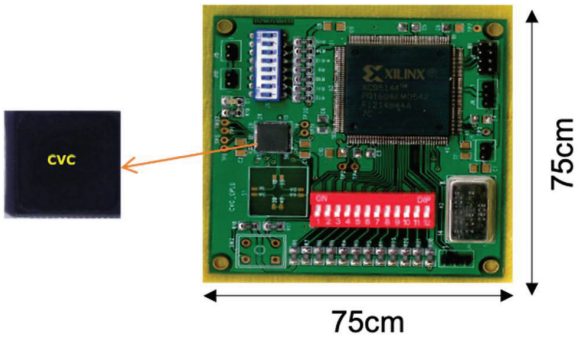


Figure 9: Application board for testing of the CVC along with accelerometer

C. CVC output characteristics vs. capacitance change

The plot shows (Figure 10) the closed-loop CVC output voltage V_{out} as a function of the accelerometer's differential capacitance change ΔC over a full-scale range of ≈0–210 fF (which corresponds to 30 g for a device with 7 fF/g. The data closely follows the fit, indicating good linearity across most of the range; the largest deviations (around ΔC≈140–170 fF) are small relative to the 4V span and are consistent with non-idealities such as finite OTA gain/bandwidth, charge-injection and clock-feedthrough in the SC network, and small ratio errors in Cs/Cf due to parasitics. The positive slope confirms correct polarity of the demodulation path, while the finite intercept reflects the expected common-mode/offset that can be trimmed digitally with the offset-capacitance bank. However, the output of the circuit showed non-linearity at specific measurement points. Current gain setting for sensitivity is 15 mV/fF (i.e., 105 mV/g), the result can be improved by ~10-20%; this can be achieved by (i) increasing C_{in}/C_f ratio in the CVC circuit or (ii) selecting a higher gain capacitance in the switched-capacitor PGA.

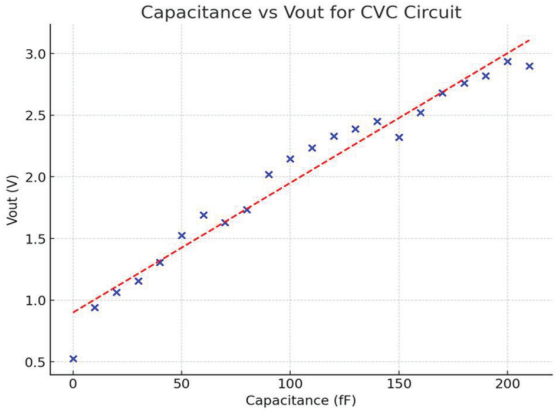


Figure 10: CVC output against the capacitance

D. Impulse Test Measurement Analysis (CVC and Accelerometer vs. Piezo Reference)

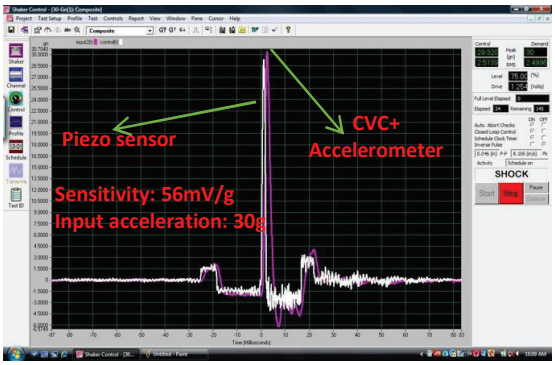


Figure 11: Impulse test measurement of CVC with commercial sensor

The displayed spectrum corresponds to an impulse (shock) test conducted on the MEMS accelerometer readout chain (CVC + accelerometer) compared against a commercial piezoelectric reference sensor on moving shaker system. The sharp central peak (as shown in Figure 11) indicates the applied impulse excitation, with both the piezo sensor (reference, yellow trace) and the CVC–accelerometer chain (magenta trace) responding concurrently.

The nearly coincident peak amplitudes confirm that the proposed CVC readout maintains high fidelity under large transient inputs, faithfully tracking the piezo sensor response. The output is programmed for sensitivity of 56 mV/g, consistent with the capacitance-to-voltage conversion relationship, and matching closely with the expected linear response for a 30 g full-scale input. The baseline noise floor remains low outside the impulse event, showing that the chopping and filtering stages suppress spurious noise contributions effectively. This result validates that the proposed interface not only performs accurately in steady-state low-g conditions but also preserves linearity and robustness under high-dynamic, shock-like accelerations—critical for deployment in robotic localization and structural monitoring applications. These results demonstrate significant improvement over conventional non-chopped architectures.

VI. Comparison With Prior Work

The proposed interface achieves low-power operation with high-g linearity, trimmed offset, and programmable gain, which addresses the limitations of prior works (as discussed in Table 2). Unlike [8], which primarily focused on reducing input-referred current noise, this work additionally ensures offset trimming and reconfigurability, thereby enhancing robustness under varying sensing conditions. Compared to [9], which demonstrated a state-of-the-art noise floor in the nano-g range but at the cost of higher power and limited programmability, the present design provides a balanced trade-off between ultra-low noise, wide bandwidth, and energy efficiency, making it more suitable for next-generation precision inertial sensing.

Table 2: Comparison with previous development

Category	This work	Royo et al., 2017 (Sensors)– Programmable low-power CVC (TIA-based)[8]	Utz et al., 2018 (IEEE Sensors J.) – Ultra-low-noise CVC + MEMS[9]
Architecture	CVC front-end, Chopper, 2nd-order LPF	Fully-differential TIA-based CVC, programmable gain & BW	Chopper/SC CVC , demodulator & filter; ultra-low-noise ROIC
Range	0-30 g	Only CVC; aimed at capacitive accel interfaces	Seismic-grade sensor (±1.5–±7 g)
Linearity	<0.1% FS	—	—
Noise density (TNEA)	System: < 570 µg/ √Hz@200Hz	~100 µg/√Hz @ 50 kHz (from 42 fA/√Hz	System: 200 ng/√Hz with >5 kHz BW; CVC ROIC: <50 zF/√Hz
Sensitivity	105 mV/g (15 mV/fF & 7fF/g)	≈4.2 mV/g (1 mV/fF; device ≈0.24 fF/g in their setup)	≈0.55 pF/g, ROIC gain configurable
Nominal Cap	1.8 pF	Targets MEMS in 0.1–few pF class	~10 pF per sense cap
Signal BW	200 Hz	Programmable 75 kHz–1.2 MHz	>5 kHz system bandwidth
Offset handling	Trim to <1 mg, correction up to 210 fF	Not a full sensor; interface-level features only	System-level temp. effect discussed; focus on noise/BW
Power / Supply	<2 mW @ 5 V, 0.35 µm CMOS	~54 µW @ 0.18 µm CMOS	~300 mW for high-precision system (sensor +ROIC)

VII. CONCLUSION

We presented a signal conditioning circuit for a 30g MEMS accelerometer designed in 350 nm CMOS process. By combining chopper-stabilized Capacitor-to-Voltage conversion with offset correction, the system achieves high resolution and stability. Stated TNEA, BW, CVC gain, and 57 aF resolution are mutually consistent as the electrical chain is well-matched. Strengths are high V/g from modest ΔC/g**,** big practical offset-trim window (210 fF)**,** simple 2nd-order LPF chain**,** and guaranteed linear 30 g operation, excellent for robust, mid-BW, single-axis applications without resorting to HV biasing or seismic-class mechanics. Future work includes better noise characteristics, large capacitance offset management (few pF), high resolution ADC integration and testing under automotive and aerospace vibration conditions.

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