Design and FPGA Realization of a High-Resolution Optical Flash Detection and Event Triggering System

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Abstract— Optical flash detection systems are essential for sensing short light pulses and triggering precise electronic systems. This paper details the design and implementation of a flash detection system using Field Programmable Gate Array (FPGA) technology. The system identifies rising-edge transitions of optical input signals (flashes) and produces accurate digital trigger pulses in response. A high-resolution timestamp counter captures the exact time of each flash, and the timestamp is sent via a UART interface for external monitoring and logging. Key modules include a flash edge detector, a 64-bit timestamp counter, and a UART transmitter. A dedicated optical fiber-compatible trigger output enables synchronization with external devices such as cameras, sensors, or data acquisition systems. The proposed architecture is simple, accurate, and suitable for real-time embedded applications in scientific research, instrumentation, and aerospace systems. Simulation results verify the timing precision and pulse generation, confirming the design's reliability and efficiency.

Keywords—FPGA, Optical Pulse Detection, High-Speed Optical Sensing, Optical Flash Detector

I. INTRODUCTION

Optical flash detection plays a vital role in time-sensitive systems such as high-speed imaging, experimental physics, and aerospace instrumentation, where short optical pulses must be detected and processed with minimal delay. Conventional microcontroller-based methods often lack the timing accuracy and predictable response required for these applications. To overcome these limitations, this work introduces an FPGA-based flash detection system capable of identifying rising-edge transitions of brief optical flashes and generating synchronized digital trigger pulses. The system achieves a deterministic response time less than 20 nanoseconds, by using a 50 MHz system clock, making it highly suitable for applications needing nanosecond-scale resolution.

The architecture integrates three core components: a flash edge detector, a 64-bit high-resolution timestamp counter, and a UART transmitter for serial data communication. Upon detecting a flash, the system records the exact timestamp of the event and transmits it externally via UART. A dedicated optical fiber-compatible trigger output enables synchronization with devices such as cameras, sensors, or data acquisition systems. Designed to be modular, efficient, and hardware-accelerated, the proposed system provides reliable performance in real-time embedded environments. Simulation results confirm its timing accuracy, functional correctness, and suitability for deployment in fast-response optical event monitoring scenarios.

II. THEORETICAL BACKGROUND

Optical flash detection systems rely on the principle of detecting transient increases in irradiance, often caused by energetic or instantaneous light-emitting events such as laser pulses, muzzle flashes, or high-speed discharges. The foundation of such detection lies in radiometric sensing, signal discrimination, and digital event handling with minimal latency.

A. Radiometric Flash Sensing

The total irradiance E received by an optical flash detector is the sum of the flash signal and background illumination:

$$\mathbf{E=Lt\cdot\Omega t+Lb\cdot(\Omega s-\Omega t)}$$

Where:

- L_t: Radiance of the flash event
- L_b: Background radiance
- Ω_t: Solid angle subtended by the flash
- Ω_s: Field of view of the detector

The electrical signal v_t generated by a photosensitive element (e.g., a photodiode) is proportional to this irradiance:

$$\boldsymbol{vt = E \cdot A0 \cdot Rg}$$

Here, A_0 is the detector's sensitive area, and Rg is the transimpedance gain of the front-end amplifier. To isolate the flash signal from ambient noise, a background subtraction is performed:

$$\boldsymbol{vs = vt - vb = (Lt - Lb) \cdot \Omega t \cdot A0 \cdot Rg}$$

This shows that the signal amplitude depends on the flash intensity, field of view, and detection gain, while being inversely influenced by background interference.

B. *Distance-Dependent Sensitivity*

The solid angle Ω_t is defined by the geometry of the flash source:

$$\Omega t = \frac{R2}{At}$$

Where A_t is the apparent area of the flash and RRR is the distance to the detector. Substituting into the earlier equation yields:

$$vs = (Lt - Lb) \cdot \frac{At\ A0\ Rg}{R^2}$$

This inverse-square relationship explains the detection range limitations — the farther the flash source, the smaller the output signal, requiring greater amplification or sensitivity for longer-range detection.

C. *Digital Edge Detection and Timing*

In digital systems, flashes are sampled at discrete clock intervals. An **edge detector** circuit identifies a flash by comparing the current and previous input values:

$$\mathbf{Trigger = flashin(t) \wedge \neg\ flashin(t-1)}$$

This Boolean condition ensures that only rising edges ($0 \rightarrow 1$) are detected, avoiding false triggering due to noise or high-level holds. The moment of detection is marked by a timestamp:

$$\mathbf{Timestamp = N \cdot Tclk}$$

Where Tclk=20 ns for a 50 MHz system clock, and N is the counter value at the moment of detection. This precise temporal encoding allows correlation with other synchronous systems.

III. Design of Components

The FPGA-based flash detector consists of four primary components: the flash detection logic, timestamp counter, UART communication module, and fiber-optic trigger output. Each module is implemented using synthesizable VHDL and designed for minimal latency, modularity, and real-time responsiveness.

A. *Flash Detector Logic*

The flash detection module captures the rising edge of the incoming *flash_in* signal, which originates from an external analog front-end (e.g., photodiode with amplifier). Internally, a 1-bit register holds the previous state of the input. On each clock cycle, the module compares the current and previous states. If a transition from '0' to '1' is observed, a 1-cycle pulse is generated on the trigger line. This ensures that only rising edges—corresponding to the start of a flash—are recognized, avoiding false detection from sustained or falling signals.

B. *Timestamp Counter*

The timestamping subsystem includes a 64-bit free-running counter clocked at 50 MHz, giving a temporal resolution of 20 ns per count. This counter continuously increments and reflects system time since power-on or reset. When a flash is detected, the current counter value is latched and passed to the UART module. The wide bit width ensures the system can operate continuously for long durations without overflow.

C. *UART Communication Module*

The UART module transmits the latched timestamp to a host system (e.g., PC or microcontroller) for logging or analysis. Data is sent in a structured format: one header byte, followed by 8 bytes representing the 64-bit timestamp, and terminated with a newline character. A finite state machine (FSM) controls the byte-wise output and ensures synchronization with UART timing, using a baud rate of 115200 bps. The transmission time per packet is approximately 0.78 ms.

D. *Fiber-Optic Trigger Output*

To allow external devices (e.g., high-speed cameras, oscilloscopes, data loggers) to react in real-time, the system generates a 20 nanosecond-wide trigger pulse on the *fiber_trigger* output. This pulse is initiated immediately after flash detection and maintained for exactly at 50 MHz, ensuring consistent synchronization timing. The signal is compatible with optical transceivers or LVTTL/CML drivers for fiber-based transmission.

IV. Model Design

The FPGA-based flash detector system focuses on a sequential signal flow that ensures precise detection, timestamping, and triggering of electronics systems by sensing a flash. The model consists of separate, modular VHDL components that carry out the following operations in a pipelined manner:

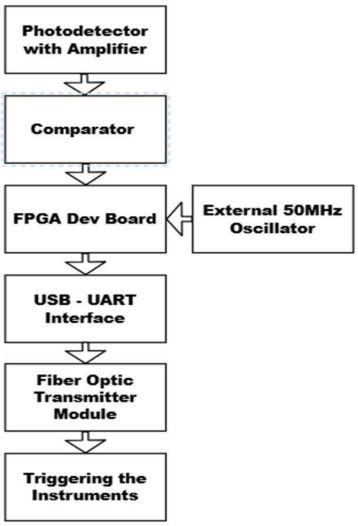

Fig 1: System architecture and working principle

V. SIMULATIONS

The functionality of the designed system, behavioral simulations were conducted using the Vivado Simulator. A comprehensive testbench was developed to simulate real-world scenarios, such as single and multiple flash events with variable time intervals. The input signal was stimulated with rising edges to mimic optical flash events, while the system's output signals were monitored in waveforms.

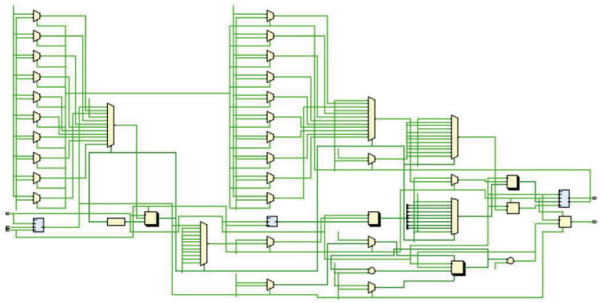

Fig 2: RTL design of the flash detector

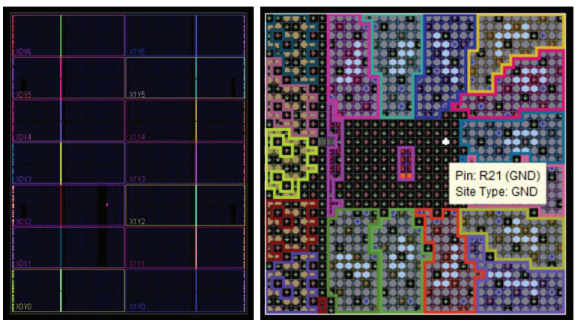

Fig 3: Implementation schematic of flash detector

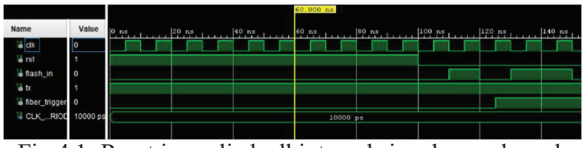

Fig 4.1: Reset is applied, all internal signals are cleared, bringing the system to a known initial state.

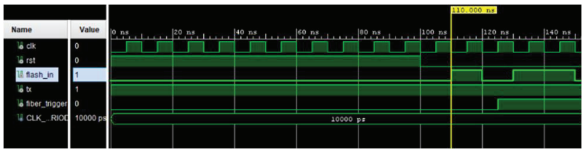

Fig 4.2: When flash_in transitions from 0 to 1, the system generates a 20 ns pulse on fiber_trigger and transmits a 64-bit timestamp via UART.

VI. RESULT ANALYSIS

The simulation of the FPGA-based flash detector system confirmed its functional correctness and reliability across various test conditions. When a valid rising edge (0 → 1) was applied to the input signal, the system successfully generated a 1 µs pulse on the output and transmitted a correctly formatted 64-bit timestamp over UART.

No trigger or UART activity was observed during conditions that lacked a valid rising edge, such as sustained high levels (1 → 1) or falling edges (1 → 0), demonstrating accurate edge detection and noise immunity. When subjected to rapid and repeated flash events with minimal spacing, the system maintained consistent operation, producing clean 20ns trigger pulses without glitches or overlap.

Furthermore, the pulse width of fiber_trigger was precisely maintained at less than 20ns, and UART packets were consistently formatted and transmitted in real time without delays or data corruption. The system also showed high stability under burst input conditions, with no loss or duplication of events, confirming its robustness for high-speed optical event detection applications.

VII. FUTURE WORK

Future improvements to the FPGA-based flash detector can enhance its functionality, scalability, and application range. One key direction is the addition of multi-channel support, enabling simultaneous detection from multiple photodiodes. This would allow spatial correlation of flash events across different locations. Another enhancement involves implementing adaptive thresholding and digital filtering to improve reliability in noisy or variable lighting conditions.

To increase data throughout and integration with modern systems, the UART interface can be upgraded to high-speed protocols such as SPI or Ethernet. Local data logging using on-chip memory can also be introduced to buffer timestamps in real time, reducing dependency on continuous transmission. Additionally, adding programmable delay and pulse width controls for the trigger output can improve compatibility with a wider range of external devices.

Finally, integrating the design into a compact, custom PCB and exploring basic on-chip flash classification logic can further transform the system into a deployable solution for field or aerospace applications.

VIII. CONCLUSION

This work successfully demonstrates the design, simulation, and verification of a high-resolution optical flash detection system implemented on an FPGA platform. The system is capable of detecting fast optical events with nanosecond-scale precision, timestamping each detected flash, and generating a synchronized less than 20ns trigger pulse suitable for controlling external instruments such as cameras or data acquisition systems. The integration of a 64-bit high-resolution timestamp counter, UART communication interface, and a fiber-compatible trigger output enables both local and remote event logging in real time.

Simulation results validated the system's reliability, functional accuracy, and timing consistency. The design accurately detected only rising edges of the input signal, effectively filtered out noise or invalid transitions, and maintained deterministic timing performance. With a measured response time of less than 20 ns and consistent UART transmission, the system proves well-suited for high-speed embedded applications in fields such as scientific instrumentation, ballistics testing, and aerospace systems.

The modular architecture and VHDL-based implementation make the system easily extendable for future enhancements such as multi-channel detection, adaptive filtering, and high-speed interfaces like SPI or Ethernet. Overall, the FPGA-based flash detector offers a robust, real-time solution for time-critical optical event monitoring.

IX. REFERENCES

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